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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,128	07/03/2003	Danny W. Wilson	03-0157 (4028-03100)	7195

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,128	WILSON ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received February 06, 2006.

- Claims 1, 6, 7, 10, 15 and 16 currently amended.
- Claims 8, 9 and 17-22 canceled.
- Claims 1-7 and 10-16 pending.

Application pending.

Response to Amendment

Applicants' arguments/amendments with respect to amended claims 1, 6, 7, 10, 15 and 16 and previously presented claims 2-5 and 11-14 filed February 06, 2006 have been considered but not persuasive. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). For example, Applicants contend the prior art of record does not teach, "a processor configured to embody a pipelined superscalar processor core."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations

from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). For example, Applicants contend the prior art of record does not teach, "an instruction prefetch unit fetches instructions and provides instructions to an instruction sequencing unit."

The Examiner disagrees with the Applicants and maintains rejections with respect to amended claims 1, 6, 7, 10, 15 and 16 and previously presented claims 2-5 and 11-14. All arguments have been considered. It is the Examiner's conclusion that amended claims 1, 6, 7, 10, 15 and 16 and previously presented claims 2-5 and 11-14, as presented, are not patentably distinct or non-obvious over the prior art of record. See prior office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

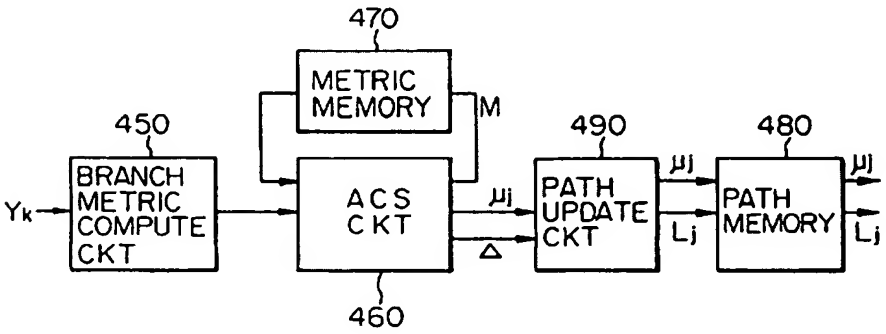
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuragawa et al. (USPN 5907586).

As per claim 1, Katsuragawa et al. (herein after: Katsuragawa) substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method

for a coding communication system are disclosed. A plurality of add compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal.

Fig. 7



Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its

estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric computing section determines the metrics of consecutive branches represented by differences between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced

at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 2, Katsuragawa substantially teaches, in view of above rejections, (figure 1) a plurality of add-compare-select circuits that feed instructions into the M break-off circuit 30.

As per claim 3, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path.

As per claims 4 and 5, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The Examiner would like to point out that a comparison has to be done between at least two add operations. The selection process follows the comparison.

As per claim 6, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the

most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 7, Katsuragawa substantially teaches, in view of above rejections, an M break-off circuit sequentially receives a plurality of path metrics sequentially detected by the plurality of Viterbi decoders during the trellis tracings, and sequentially breaks off the trellis tracings of, among the plurality of paths, unlikely paths to thereby detect M most probable paths over at least two of the plurality of Viterbi decoders. A decision circuit performs the final decision with the path metrics of the M paths to thereby determine which of the decoded signals output from the plurality of Viterbi decoders has a correct code rate.

As per claim 10, Katsuragawa substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric

compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric

computing section determines the metrics of consecutive branches represented by differences between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 11, Katsuragawa substantially teaches, in view of above rejections, (figure 1) a plurality of add-compare-select circuits that feed instructions into the M break-off circuit 30.

As per claim 12, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path.

As per claims 13 and 14, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The Examiner would like to point out that a comparison has to be done between at least two add operations. The selection process follows the comparison.

As per claim 15, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 16, Katsuragawa substantially teaches, in view of above rejections, an M break-off circuit sequentially receives a plurality of path metrics sequentially detected by the plurality of Viterbi decoders during the trellis tracings, and sequentially breaks off the trellis tracings of, among the plurality of paths, unlikely paths to thereby detect M most probable paths over at least two of the plurality of Viterbi decoders. A decision circuit performs the final decision with the path metrics of the M paths to thereby determine which of the decoded signals output from the plurality of Viterbi decoders has a correct code rate.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
April 18, 2006

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